

## 14 Timer (ARM side)

### 14.1 Introduction

The ARM Timer is *based* on a ARM AP804, but it has a number of differences with the standard SP804:

- There is only one timer.
- It only runs in continuous mode.
- It has a extra clock pre-divider register.
- It has a extra stop-in-debug-mode control bit.
- It also has a 32-bit free running counter.

The clock from the ARM timer is derived from the system clock. This clock can change dynamically e.g. if the system goes into reduced power or in low power mode. Thus the clock speed adapts to the overall system performance capabilities. For accurate timing it is recommended to use the system timers.

### 14.2 Timer Registers:

The base address for the ARM timer register is 0x7E00B000.

Address offset <sup>8</sup>	Description
0x400	Load
0x404	Value (Read Only)
0x408	Control
0x40C	IRQ Clear/Ack (Write only)
0x410	RAW IRQ (Read Only)
0x414	Masked IRQ (Read Only)
0x418	Reload
0x41C	<i>Pre-divider (Not in real 804!)</i>
0x420	<i>Free running counter (Not in real 804!)</i>

### Timer Load register

The timer load register sets the time for the timer to count down. This value is loaded into the timer value register after the load register has been written or if the timer-value register has counted down to 0.

<sup>8</sup> This is the offset which needs to be added to the base address to get the full hardware address.



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## Timer Value register:

This register holds the current timer value and is counted down when the counter is running. It is counted down each timer clock until the value 0 is reached. Then the value register is re-loaded from the timer load register and the interrupt pending bit is set. The timer count down speed is set by the timer pre-divide register.

## Timer control register:

The standard SP804 timer control register consist of 8 bits but in the BCM implementation there are more control bits for the extra features. Control bits 0-7 are identical to the SP804 bits, albeit some functionality of the SP804 is not implemented. All new control bits start from bit 8 upwards. Differences between a real 804 and the BCM implementation are shown in italics.

Name: Timer control		Address: base + 0x40C	Reset: 0x3E0020
Bit(s)	R/W	Function	
31:10	-	<Unused>	
23:16	R/W	Free running counter pre-scaler. Freq is $sys\_clk/(prescale+1)$ <i>These bits do not exists in a standard 804! Reset value is 0x3E</i>	
15:10	-	<Unused>	
9	R/W	0 : Free running counter Disabled 1 : Free running counter Enabled <i>This bit does not exists in a standard 804 timer!</i>	
8	R/W	0 : Timers keeps running if ARM is in debug halted mode 1 : Timers halted if ARM is in debug halted mode <i>This bit does not exists in a standard 804 timer!</i>	
7	R/W	0 : Timer disabled 1 : Timer enabled	
6	R/W	<i>Not used, The timer is always in free running mode. If this bit is set it enables periodic mode in a standard 804. That mode is not supported in the BC2835M.</i>	
5	R/W	0 : Timer interrupt disabled 1 : Timer interrupt enabled	
4	R/W	<Not used>	
3:2	R/W	Pre-scale bits: 00 : pre-scale is clock / 1 (No pre-scale) 01 : pre-scale is clock / 16 10 : pre-scale is clock / 256 11 : pre-scale is clock / 1 ( <i>Undefined in 804</i> )	
1	R/W	0 : 16-bit counters 1 : 23-bit counter	
0	R/W	<i>Not used, The timer is always in wrapping mode. If this bit is set it enables one-shot mode in real 804. That mode is not supported in the BCM2835.</i>	



## Timer IRQ clear register:

The timer IRQ clear register is write only. When writing this register the interrupt-pending bit is cleared.

When reading this register it returns 0x544D5241 which is the ASCII reversed value for "ARMT".

## Timer Raw IRQ register

The raw IRQ register is a read-only register. It shows the status of the interrupt pending bit.

Name: Raw IRQ		Address: base + 0x40C	Reset: 0x3E0020
Bit(s)	R/W	Function	
31:0	R	0	
0	R	0 : The interrupt pending bits is clear 1 : The interrupt pending bit is set.	

The interrupt pending bits is set each time the value register is counted down to zero. The interrupt pending bit can not by itself generates interrupts. Interrupts can only be generated if the interrupt enable bit is set.

## Timer Masked IRQ register:

The masked IRQ register is a read-only register. It shows the status of the interrupt signal. It is simply a logical AND of the interrupt pending bit and the interrupt enable bit.

Name: Masked IRQ		Address: base + 0x40C	Reset: 0x3E0020
Bit(s)	R/W	Function	
31:0	R	0	
0	R	0 : Interrupt line not asserted. 1 :Interrupt line is asserted, (the interrupt pending and the interrupt enable bit are set.)	

## Timer Reload register:

This register is a copy of the timer load register. The difference is that a write to this register does not trigger an immediate reload of the timer value register. Instead the timer load register value is only accessed if the value register has finished counting down to zero.

## The timer pre-divider register:

Name: pre-divide		Address: base + 0x41C	Reset: 0x07D
Bit(s)	R/W	Function	
31:10	-	<Unused>	
9:0	R/W	Pre-divider value.	

The Pre-divider register is not present in the SP804.



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The pre-divider register is 10 bits wide and can be written or read from. This register has been added as the SP804 expects a 1MHz clock which we do not have. Instead the pre-divider takes the APB clock and divides it down according to:

$$\text{timer\_clock} = \text{apb\_clock}/(\text{pre\_divider}+1)$$

The reset value of this register is 0x7D so gives a divide by 126.

### **Free running counter**

Name: Free running		Address: base + 0x420	Reset: 0x000
Bit(s)	R/W	Function	
31:0	R	Counter value	

The free running counter is not present in the SP804.

The free running counter is a 32 bits wide read only register. The register is enabled by setting bit 9 of the Timer control register. The free running counter is incremented immediately after it is enabled. The timer can not be reset but when enabled, will always increment and roll-over. The free running counter is also running from the APB clock and has its own clock pre-divider controlled by bits 16-23 of the timer control register.

This register will be halted too if bit 8 of the control register is set and the ARM is in Debug Halt mode.